



AMG (Analog and MEMS Group)

General Purpose Analog & RF Division

Power Management

Quality and Reliability

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Reliability Evaluation Report

On Technology HBIP40

T.V.:

LM317LD13TR Pkg SO8 STS

LM317LZ-TRL Pkg TO92 ASE

Product Lines	<i>AL1701</i>
Product Description	Low current 1.2 to 37 V adj Vreg <i>1.2 V to 37 V adjustable voltage regulators</i>
P/N	<i>LM317LD13TR</i> <i>LM317Z-TRL</i>
Product Group	<i>AMG</i>
Product division	<i>GENERAL PURPOSE ANALOG & RF</i>
Package	<i>-SO8 TO92</i>
Silicon Process technology	<i>HBIP40</i>

Locations	
Wafer fab	SINGAPORE Ang Mo Kio
Assembly site	Shenzhen / ASE
Reliability Lab	Catania
Reliability assessment	

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	November 2019	6	Angelo Basile	Giuseppe Giacobello	Final Report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification New Product LM317LD13TR and the LM317LZ-TR in HBIP40 technology assembled in SO8 Shenzhen and TO92 ASE Subcontractor.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests has how that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime

The present reliability results are positive.



DEVICE CHARACTERISTICS

3.3 Device description

The LM217 LM317 are monolithic integrated circuits in TO-220, TO-220FP and D²PAK packages intended for use as positive adjustable voltage regulators. They are designed to supply more than 1.5 A of load current with an output voltage adjustable over a 1.2 to 37 V range. The nominal output voltage is selected by means of a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed regulators

3.4 Construction note

	P/N - LM317LZ-TR	P/N LM317LD13TR
Wafer/Die fab. information		
Wafer fab manufacturing location	SINGAPORE Ang Mo Kio	
Technology	HBIP40V	
Die finishing back side	Lapped silicon	
Die size	980x960 micron	980x960 micron
Passivation type	P-VAPOX/NITRIDE	
Wafer Testing (EWS) Information		
Electrical testing manuf.	Ang M0o Kio EWS	
Assembly information		
Assembly site	ASE	SHENZHEN
Package description	TO92	SO8
Molding Compound	EPOXY	
Die Attach Material	EPOXY	
Wires Bonding Mat.	WIRE Cu 1mils	



4 TESTS RESULTS SUMMARY

4.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	V67209TN	GK8110M401	GK8110M4	SO8	AL1701	
2	V67209TN	A1936NUZ	GE936063	TO92	AL1701	

4.2 Test plan and results summary

Test		Std ref.	Conditions	SS	Steps	Failure/SS		Note
						Lot 1 SO8	Lot 2 TO92	
Die Oriented Tests								
HTOL	N	JESD22 A-108	Ta = 125°C, BIAS 40 V	77	168 h	0/77	0/77	
					500 h	0/77	0/77	
					1000 h	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C	45	168 h	0/45		
					500 h	0/45		
					1000 h	0/45		
Package Oriented Tests								
PC		JESD22-A113	Drying 24 H @ 125°C Store 168h @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass		
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	77	168 h	0/77		
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	77	100 cy	0/77		
					200 cy	0/77		
					500 cy	0/77		
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS 24V	77	168 h	0/77	0/77	
					500 h	0/77	0/77	
					1000 h	0/77	0/77	
Others Test								
ESD	N	ANSI / ESDA JEDEC JS-001	HBM	3	+/- 1000V	Pass		
		ANSI/ESDA JEDEC JS002	CDM	3	+/- 500V			

4.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Test		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. HBM: Human Body Model CDM: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.